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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,075	09/17/2003	Seung-Hwan Moon	6192.0313.US	5051

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EXAMINER
AMADIZ, RODNEY

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,075	MOON, SEUNG-HWAN	
	Examiner	Art Unit	
	Rodney Amadiz	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1-3 and 9-13* is/are rejected.

7)☒ Claim(s) *4-8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. 6,359,607) in view of Kawaguchi et al. (U.S. Patent 6,118,421).

As to **Claim 1**, Yanagi et al. teaches a liquid crystal display comprising: a liquid crystal panel including a gate line ***(Fig. 9, Reference Character G(M))***, a data line ***(Fig. 9, Reference Character S(N))***, and a pixel including a switching element connected to the gate line and the data line ***(Fig. 9, Reference Characters g(i,j), T(i,j) and P(i,j))***; a gate driver applying a gate signal for controlling the switching element to the gate line ***(Fig. 9, Reference Number 300)***; and a data driver ***(Fig. 9, Reference Number 300)***, wherein the gate signal includes a gate-on voltage for turning on the switching element and a gate-off voltage for turning off the switching element and the gate-on voltage has at least two different levels ***(See Fig. 5, waveform VG(j) and Col. 10, lines 20-30, Col. 15, lines 45-50, Col. 16, line 56—Col. 17, line 4, Col. 17, lines 48-58 and Col. 18, lines 29-65)***. Yanagi et al. does not teach the data driver selecting gray voltages corresponding to gray signal and applying the selected gray voltages to the data line. Examiner cites Kawaguchi et al. to teach a data driver selecting gray voltages corresponding to gray signals and applying the selected gray voltages to the data line ***(Fig. 8A, Reference Numbers 104 and 102).*** At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a gray

scale voltage generator as taught by Kawaguchi et al. in the liquid crystal display taught by Yanagi et al. in order to enhance picture quality.

As to **Claim 2**, Yanagi et al. teaches the gate-on voltage continuously varying for a predetermined ***time (See Fig. 5, waveform VG(j) and notice the gate-on voltage varying (Vslope))***.

As to **Claim 3**, Yanagi et al. teaches two levels including a first level ***(Fig. 5, waveform VG(j)-top of Vslope)*** and a second level lower than the first level ***(Fig. 5, waveform VG(j)-bottom of Vslope)*** and the gate-on voltage continuously decreases from the first level to the second level for the predetermined time ***(See Fig. 5, waveform VG(j) and notice the downward slope of Vslope).***

2. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. and Kawaguchi et al. in view of Cochran (U.S. Patent 3,114,112).

As to **Claim 9**, the modified circuit of Yanagi et al. and Kawaguchi et al. fail to teach a voltage generator including: a first switch selectively transmitting a first voltage; a first capacitor connected to the first switch and charging a voltage from the first switch; and a second switch connected to the first capacitor and forming a discharging path of the voltage charged in the first capacitor. Examiner cites Cochran to teach a voltage generator including: a first switch selectively transmitting a first voltage ***(Fig. 1, Reference Number 31)***; a first capacitor connected to the first switch and charging a voltage from the first switch ***(Fig. 1, Reference Number 33)***; and a second switch connected to the first capacitor and forming a discharging path of the voltage charged in

the first capacitor ***(Fig. 1, Reference Number 37)***. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporate a voltage generator as taught by Cochran in the liquid crystal display taught by Yanagi et al. in order to accurately provide the voltage necessary to have the liquid crystal display device function properly.

As to **Claim 10**, the modified circuit of Yanagi et al. Kawaguchi et al. and Cochran teach the voltage generator further comprising a resistor connected between the second switch and the first capacitor and the first switch discharges according to a time constant determined by a resistance of the resistor and a capacitance of the capacitor ***(Cochran—Fig. 1, Reference Number 27)***.

As to **Claim 11**, the modified circuit of Yanagi et al. Kawaguchi et al. and Cochran teach the voltage generator further comprising: a signal generator for generating a pulse signal with a predetermined period ***(Cochran—Fig. 1, Reference Number 9)***; a voltage divider diving the first voltage ***(Cochran—Fig. 1, Reference Numbers 19 and 23)***; and a second capacitor for charging a voltage from the voltage divider for turning on and turning off the first switch responsive to the pulse signal from the signal generator, wherein the first switch and the second switch are alternately activated based on the pulse signal from the signal generator ***(Cochran—Fig. 1, Reference Numbers 45)***.

As to **Claim 12**, the modified circuit of Yanagi et al. Kawaguchi et al. and Cochran teaches the first switch comprising a NPN bipolar transistor and the second switch comprising a PNP bipolar transistor. Yanagi et al. Kawaguchi et al. and

Cochran; however, do not teach the first switch comprising a PNP bipolar transistor and the second switch comprising an NPN bipolar transistor. Official notice is taken that it is well known to exchange NPN transistors with PNP transistors in a circuit as long as the logic of the circuit is reserved. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to swap the transistors in the liquid crystal display taught by the combination of Yanagi et al. Kawaguchi et al. and Cochran because the circuit would perform the same function.

As to **Claim 13**, the modified circuit of Yanagi et al. Kawaguchi et al. and Cochran teaches the signal generator is connected to a base of the PNP bipolar transistor and is connected to a base of the NPN bipolar transistor via the first capacitor ***(Cochran—Fig. 1, Reference Number 9 is connected to 37 and 31 through lines 35 and 29).***

Allowable Subject Matter

3. **Claims 4-8 and 14** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. **Claim 15** is allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: As to **Claim 15** the above cited references have failed to teach "generating a plurality of pairs of a positive gray voltage (V^+) and a negative gray voltage (V^-) for respective grays satisfying $(V^+ + V^-) / 2 = Vconst$, where Vconst is a

predetermined value; generating a gate signal including a gate-on voltage for turning on the switching element and a gate-off voltage for turning off the switching element; applying the gate signal to the gate lines; and applying the gray signals to the data lines, wherein the gate-on voltage decreases from a first level (Von1) to a second level (Von2) for a predetermined time and ((Von1 + Vconst) / 2 – (Von1 + Vconst) / 2 x 10 %) ≤ Von2 ≤ ((Von1 + Vconst) / 2 + (Von1 + Vconst) / 2 x 10 %).", as claimed.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney Amadiz whose telephone number is (571) 272-7762. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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